TRANSMITTAL

Electronic Version v1.1

Stylesheet Version v1.1.0

Title of
Invention

ACCURATE TIMING ANALYSIS OF INTEGRATED CIRCUITS WHEN COMBINATORIAL LOGIC OFFERS A LOAD

Application Number :

Date

Mr. Somasekar JAYARAMAN

First Named Applicant: Confirmation Number:

Attorney Docket Number: TI-37107

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Submitted By:	Elec. Sign.	Sign. Capacity
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Documents being submitted:	Files
us-fee-sheet	txnefiling-usfees.xml
	us-fee-sheet.xsl
	us-fee-sheet.dtd
us-request	txnefiling-usrequ.xml
	us-request.dtd
	us-request.xsl
us-declaration	decltxn93.tif
application-body	spectxn93-trans.xml
,	us-application-body.xsl
	application-body.dtd
	wipo.ent
	mathml2.dtd
	mathml2-qname-1.mod
	isoamsa.ent
	isoamsb.ent
	isoamsc.ent
	isoamsn.ent
	isoamso.ent
	isoamsr.ent
	isogrk3.ent
	isomfrk.ent
	isomopf.ent
	isomscr.ent
	isotech.ent
	isobox.ent
	isocyr1.ent
	isocyr2.ent
	isodia.ent
	isolat1.ent
	isolat2.ent
	isonum.ent
	isopub.ent
	mmlextra.ent
	mmlalias.ent
	soextblx.dtd
	fig_1.tif
	fig_2.tif
	fig_3.tif
	fig_4.tif
	fig_5.tif
	fig_6.tif
	fig_7.tif
Comments	

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